Docket No.: SON-2047
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko Koh et al.

Application No.: 09/802,857 | Confirmation No.: 3304

Filed: March 12, 2001 | Art Unit: 2192

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM | Examiner: M. J. Yigdall

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on May 23, 2011.

Fees-general authorization

If any additional fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

New issues, if any

Regarding any new issue raised in the Reply Brief, if present, U.S. patent practice and procedures set forth within 37 C.F.R. §41.43(a)(1) instructs as follows:

> After receipt of a reply brief in compliance with § 41.41, the primary examiner must acknowledge receipt and entry of the reply brief. In addition, the primary examiner may withdraw the final rejection and reopen prosecution or may furnish a supplemental examiner's answer responding to any new issue raised in the reply brief.

Arguments in the Appeal Brief are incorporated by reference

All arguments presented within the Appeal Brief of March 10, 2011 are incorporated herein by reference.

Additional arguments are provided hereinbelow

Among others, the following positions were presented in the Examiner's Answer, each of which will be addressed in turn in this Reply Brief beginning on page 3 of this paper.

REMARKS

i. Standards for review.

The Board is required to set forth in its opinions specific findings of fact and conclusions of law adequate to form a basis for appellate review. *Gechter v. Davidson*, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997) (*Decision of the Board vacated and remanded for specific findings of fact and conclusions of law adequate to form a basis for appellate review*).

ii. Grouping of claims presented in the Appeal Brief.

There is no *carte blanche* by the Board to ignore the distinctions between separate grounds of rejection and to select the broadest claim rejected on one ground. *In re McDaniel*, 293 F.3d 1379, 63 USPQ2d 1462 (Fed. Cir. 2002).

A. U.S. patent practice and procedures pursuant to 37 C.F.R. §41.37(c)(1)(vii) provides in part:

Any claim argued separately should be placed under a subheading identifying the claim by number.

Claims argued as a group should be placed under a subheading identifying the claims by number.

iii. Appellant hereby appeals the final rejection of claims 63-69.

Appeal to the Board may include arguments and/or evidence to show that the examiner made an error in either (a) An underlying finding of fact upon which the final conclusion of obviousness was based, or (b) Reasoning used to reach the legal conclusion of obviousness. *Ex Parte Frye*, 94 USPQ2d 1072, 1075, (Bd. Pat. App. & Int. 2010).

A. Advisory Action of May 18, 2011.

The Advisory Action indicates ***entry*** of the Amendment in Response to Final Office Action Under 37 C.F.R. 1.116 filed on March 10, 2011.

B. Claims on appeal.

On appeal are claims 63-69, which are presented hereinbelow in the Claims Appendix.

iv. Claim rejections.

A. Rejection of claim 63 under 35 U.S.C. §112, second paragraph.

1. For this rejection only, claim 63 stands or falls alone.

Page 2 of the Advisory Action indicates the ***withdrawal*** of this rejection.

Accordingly, the rejection of claim 63 under 35 U.S.C. §112, second paragraph, is *no longer the subject of this appeal*.

B. Rejection of claims 53, 55-59 and 64-69 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,784,537 (Suzuki).

1. For this rejection only, claims 53, 55-59 stand or fall together.

The Amendment After Final Office Action Under 37 C.F.R. 1.116 includes the cancellation of claims 53 and 55-59.

As a consequence, prior claims 53 and 55-59 are *no longer the subject of this appeal*.

2. For this rejection only, claims 64-65 stand or fall together.

Claim 64 has claim 65 dependent thereon. The Examiner's Answer maintains this rejection of claims 64-65.

Claim 64 is drawn to a data processing apparatus comprising:	
a central processing unit (10) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (S_A), a first signal (S_{A1}) and a second signal (S_{A2}) being input to said central processing unit (10) as said interrupt request signal (S_A),	Paragraph beginning at page 24, line 25.
wherein said central processing unit (10) executes a program code, said program code being stored in memory at a program address,	Paragraph beginning at page 15, line 18.
wherein said first signal (S_{A1}) indicates when said program address and a first bug address coincide, said second signal (S_{A2}) indicating when said program address and a second bug address coincide.	Paragraph beginning at page 24, line 21.

a) Page 10 of the Examiner's Answer asserts the following:

> ***However, in Suzuki, the interruption request signal 34 is generated a plurality of times. Suzuki describes that the interruption request signal 34 is generated S number of times for the S number of correcting portions in a program module (see, e.g., step S5 in FIG. 4A; steps S28, S29 and S30 in FIG. 4B; column 6, lines 27-36 and column 6, line 65 to column 7, line 2). In other words, S number of interruption request signals 34 are input to the CPU 14.***

In response, it is well settled that obviousness requires a suggestion of all limitations in a claim. *Ex parte Bedoukian*, Appeal No. 2010-007177, pg. 3, (BPAI, March, 2011).

Specifically, the Patent and Trademark Office determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "***in light of the specification as it would be interpreted by one of ordinary skill in the art***". *Phillips v. AWH Corp.*, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005).

On the other hand, it is improper to read a limitation from the specification into the claims. *Liebel-Flarsheim Co. v. Medrad Inc.*, 69 USPQ2d 1801, 1806 (Fed. Cir. 2004). The claim must stand or fall upon the elements recited therein. In re Casey, 152 USPQ 235, 237 (C.C.P.A. 1967).

Here, there is a cooperative relationship between the various elements in the claims on appeal. *Illinois Tool Works, Inc. v. Continental Can Company, Inc.*, 154 USPQ 401, 420-21 (N.D. Ill. 1967).

The plain meaning of claims language is entitled to a strong presumption that it correctly expresses the scope of the claim. *In re Certain Thermometer Sheath Packages*, 205 USPQ 932, 941 (ITC 1979).

In this regard, claim 64 includes a central processing unit (10) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (S_A), a

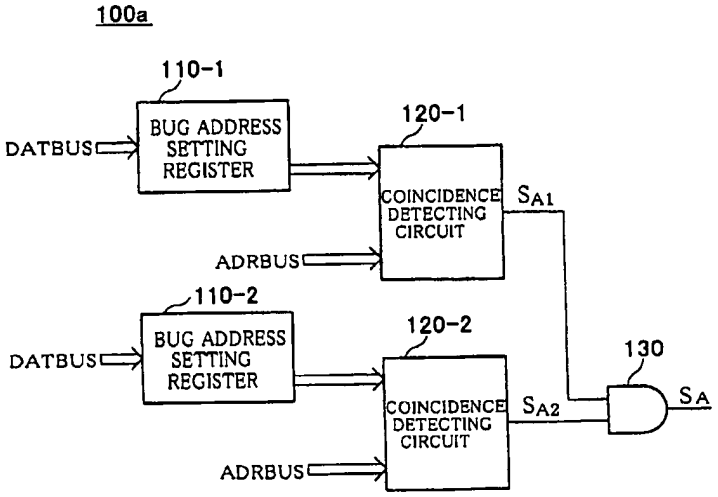
first signal (S_{A1}) and a second signal (S_{A2}) being input to said central processing unit (10) as said interrupt request signal (S_A).

Nevertheless, the claimed interrupt request signal being a single signal occurring multiple times as contended within the Examiner's Answer on page 10.

In response, the specification is the single best guide to the meaning of a disputed term. *In re Translogic Technology Inc.*, 84 USPQ2d 1929, 1935 (Fed. Cir. 2007).

Words that were defined in the specification must be given the same meaning when used in the claims. *McGill Incorporated v. John Zink Company*, 221 USPQ 944, 949 (Fed. Cir. 1984).

Figure 7 of the specification for the claims on appeal is provided hereinbelow.



The specification for the claims on appeal provides the following beginning at page 24, line 21.

> The coincidence detecting circuits 120-1 and 120-2 compare the two bug addresses with a program address. When addresses coincide, they output *low level signals SA1 and SA2, **respectively***.

The specification for the claims on appeal provides the following beginning at page 24, line 25:

> When there is sufficient leeway in the interrupt processing of the CPU 10, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 can be input to the CPU 10 as two different interrupt request signals. Accordingly, the CPU 10 receives these as different interrupt requests and executes the debugged programs separately to correct the two bugs. In general, however, the number of the interruptions that the CPU 10 is able to process is limited, so *a plurality of bug processings have to be assigned to a single interruption*. In this case, as shown in FIG. 7, *the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 are input to an AND gate 130, and the* ***output signal S_A of the AND gate 130 is input to the CPU 10 as the interrupt request signal***.

Claim 64 provides for a ***single*** interrupt request signal (S_A) being a combination of ***two*** signals (*first signal (S_{A1}) and second signal (S_{A2})*).

It is axiomatic that, in proceedings before the PTO, claims in an application are to be given their broadest reasonable interpretation consistent with the specification, and that ***claim language should be read in light of the specification*** as it would be interpreted by one of ordinary skill in the art. *In re Bond*, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990).

Since it would be ***unreasonable*** *for the PTO* ***to ignore*** *any interpretive guidance afforded by the applicant's written description*, either phrasing connotes the same notion: as an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification. *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

The statutory basis for the rejection of claims 64-65 is ***anticipation*** under 35 U.S.C. §102.

Regarding a rejection based upon ***anticipation***, *Yorkey v. Diab*, 94 USPQ2d 1444, 1447 (Fed. Cir. 2010) explains that determination that a claim is ***anticipated*** under 35 U.S.C. §102(b) involves two analytical steps:

1. An interpretation of the claim language; and

2. A comparison of the construed claim to a prior art reference and make factual findings that ***each and every*** limitation is found either ***expressly or inherently*** in that ***single prior art reference***.

However, Suzuki ***fails*** to ***expressly*** disclose each an every claimed feature at least for the reasons provided hereinabove.

The fact that a certain result or characteristic may occur or be present in the prior art is ***not sufficient to establish the inherency*** of that result or characteristic. *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

The mere fact that a certain thing ***may result*** from a given set of circumstances ***is not sufficient*** *to show an inherent* ***anticipation***. *Continental Can Co. v. Monsanto Co.*, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

However, Suzuki also ***fails*** to ***inherently*** disclose each an every claimed feature at least for the reasons provided hereinabove.

As a consequence, each an every claimed feature ***can not*** *be found within Suzuki.*

Thus, Suzuki ***fails to anticipate*** the claims on appeal.

3. For this rejection only, claim 66 stands or falls alone.

The Examiner's Answer maintains this rejection of claim 66.

Claim 66 is drawn to a data processing apparatus as set forth in claim 65, wherein a second coincidence detecting circuit (120-2) compares said program address with said second bug address, said second coincidence detecting circuit (120-2) outputting said second signal (S_{A2}) when said program address and said second bug address coincide.	Paragraph beginning at page 24, line 21.

a) Incorporation by reference.

For the purposes of brevity, the arguments presented hereinabove with respect to claim 64 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

b) Page 11 of the Examiner's Answer asserts the following:

Suzuki clearly teaches a coincidence detecting circuit in the form of ROM correction processing circuit 24 (see, e.g., FIG. 1 and column 4, lines 12-26). Here, Appellant contends that Suzuki "fails to depict the ROM correction processing circuit 24 having more than one PC comparison register section 20" and that instead, "only a single PC comparison register section 20 is disclosed" (brief, page 13).

However, in Suzuki, the ROM correction processing circuit 24 also includes a PC value latch section 22. To generate the S number of interruption request signals 34 noted above, Suzuki further describes that the PC value latch section 22 is updated S number of times for the S number of correcting portions in the program module

(see, e.g., step S6 in FIG. 4A; steps S28, S29 and S30 in FIG. 4B; column 6, lines 6-11 and column 7, lines 2-7). In other words, Suzuki teaches S number of instances of the ROM correction processing circuit 24.

In response, although the PTO must give claims their broadest reasonable interpretation, this ***interpretation must be consistent with the one that those skilled in the art would reach***. *In re Cortright*, 49 USPQ2d 1464, 1467 (Fed. Cir. 1999).

Here, claim 65 is drawn to a data processing apparatus as set forth in claim 64, wherein a first coincidence detecting circuit (120-1) compares said program address with said first bug address, said first coincidence detecting circuit (120-1) outputting said first signal (S_{A1}) when said program address and said first bug address coincide.

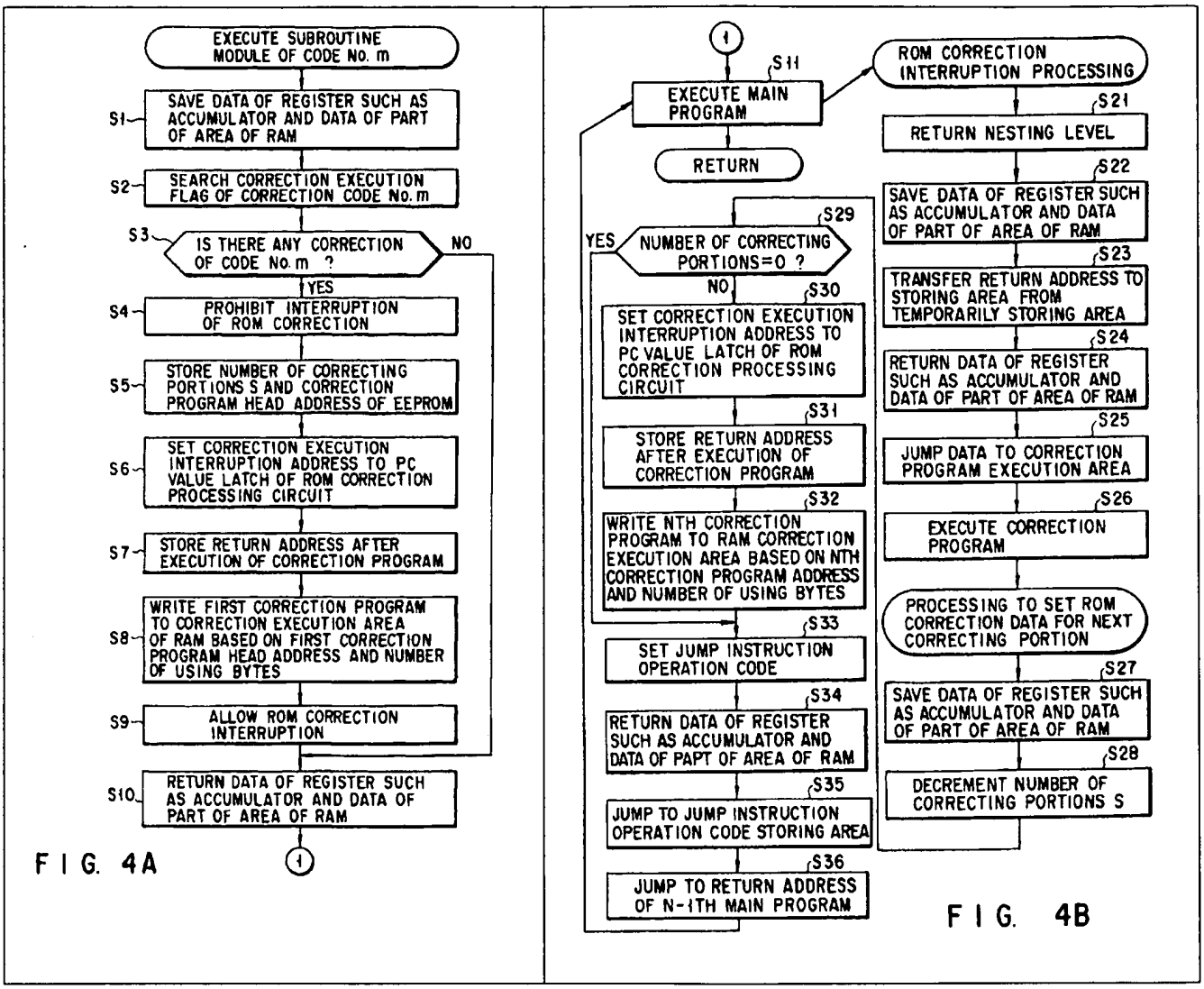
Being dependent upon claim 65, ***claim 66*** is drawn to a data processing apparatus ***as set forth in claim 65***, wherein a second coincidence detecting circuit (120-2) compares said program address with said second bug address, said second coincidence detecting circuit (120-2) outputting said second signal (S_{A2}) when said program address and said second bug address coincide.

Referring to Figure 7 of the specification for the claims on appeal, the ***coincidence detecting circuits 120-1 and 120-2*** compare the two bug addresses with a program address (specification at page 24, lines 21-22).

However, the circuitry disclosed in Suzuki is incapable of simultaneously comparing ***two*** bug addresses with a ***single*** program address.

The statutory basis for the rejection of claims 64-65 is ***anticipation*** under 35 U.S.C. §102.

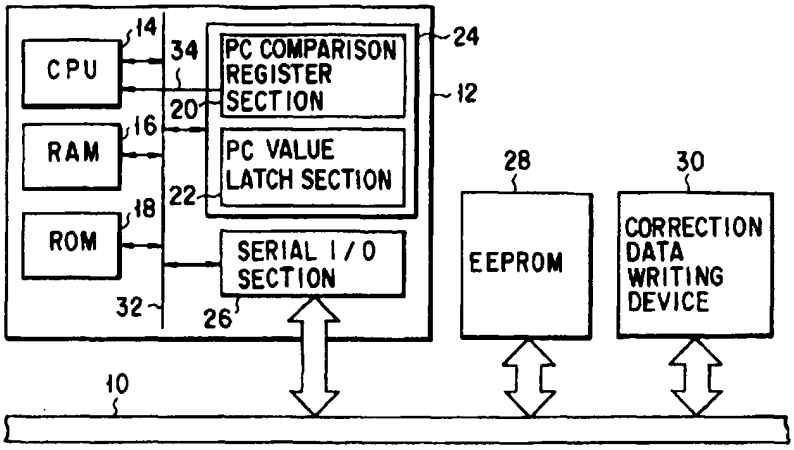
In this regard, Figures 4A and 4B of Suzuki are provided hereinbelow.



However, Figures 4A and 4B of Suzuki ***fail*** to show a ***structure*** having ***two*** coincidence detecting circuits.

Specifically, Figures 4A and 4B of Suzuki are ***flow charts*** explaining an operation when a sub-routine mode of a code No. m of the microcomputer of Figure 1 is executed (Suzuki at column 3, lines 11-14).

Figure 1 of Suzuki is provided hereinbelow.



The microcomputer 12 comprises a CPU 14, a RAM 16, a ROM 18, a ***PC (program counter) comparison register section 20***, a ROM correction processing circuit 24 having a ***PC value latch section 22***, and a serial i/O section 26 (Suzuki at column 3, lines 59-63).

Suzuki arguably discloses that the PC comparison register section 20 of the ROM correction processing circuit 24 compares a value stored in the PC latch section 22 with an address value (program counter value) of the internal bus 32 (Suzuki at column 4, lines 12-16).

Whereas Suzuki arguably discloses a ***single*** PC comparison register section 20, ***more than one*** PC comparison register section 20 is ***not disclosed*** within Suzuki.

Whereas Suzuki arguably discloses a ***single*** PC latch section 22, ***more than one*** PC latch section 22 is ***not disclosed*** within Suzuki.

The protocol of giving claims their broadest reasonable interpretation during examination ***does not include giving claims a legally incorrect interpretation***. *In re Skvorecz*, 92 USPQ2d 1020, 1024 (Fed. Cir. 2009)(*Board erred in holding that some wire legs of the Skvorecz device, as claimed, need not have an offset, when the claims state that each wire leg has an offset*).

Here, Suzuki discloses the following at column 4, lines 1-26:

> The RAM 16 is used as a working area for temporarily saving intermediate processing data of, e.g. calculation, or for storing an adjustment value (including a flag) transferred from the EEPROM 28 when the program is actually executed. In the data communication through the serial i/O bus 10, the serial i/O section 26 receives/transmits serial data having 8 to 16 bits per unit word from/to an EEPROM 28 or the correction data writing device 30.
>
> At this time, received/transmitted data is stored in the RAM 16 and the PC value latch section 22 of the ROM correction processing circuit 24 through the internal bus 32 of the microcomputer 12 as required. ***The PC comparison register section 20 of the ROM correction processing circuit 24 compares a value stored in the PC latch section 22 with an address value (program counter value) of the internal bus 32***. Then, if these values are consistent with each other, the PC comparison register section 20 outputs an interruption request signal 34 to the CPU 14. Therefore, if an arbitrary address value for interruption processing is set in the PC value latch section 22 of the ROM correction in advance, interruption processing can be automatically executed to the CPU 14 when the value of the program counter is equal to the value of the PC value latch section 22. In other words, if one ROM correction processing circuit 24 is provided, it is possible to execute the program other than the ROM 18 while the program of the ROM 18 is executing.

Here, only a ***single*** PC comparison register section 20 is disclosed in Suzuki.

Regarding Figure 4B, Suzuki arguably discloses the following at column 6, lines 27-36:

> In ***step S11***, the main program of the subroutine module of the code No. m is executed at the first time. If the correction execution interruption address set in step S6 is accessed by PC (not shown) during the execution of the main program, ***the PC comparison register section 20 generates a ROM correction interruption request to***

> ***the CPU 14***. The CPU 14 moves the processing to step 21 to execute the ROM correction interruption processing on the receipt of the request.

Here, only a ***single*** PC comparison register section 20 is disclosed in Suzuki.

Page 11 of the Examiner's Answer further asserts that *Suzuki teaches S number of instances of the ROM correction processing circuit 24.*

In response, Suzuki arguably discloses that the above-obtained ***number of correction S*** of code No. m and the head address ("0 xx (H)") of the ROM correction data area are stored (step S5)(Suzuki at column 6, lines 3-5).

Here, the Examiner's Answer ***fails*** to show that the skilled artisan would have considered the *number of correction S of code No. m* to have been plural coincidence detecting circuits. See *Ex parte Darolia*, Appeal No. 2009-005819, pgs. 7-8, (BPAI, June, 2010)(*Examiner's rejection **reversed**: Examiner has not directed Board to any disclosure within the reference*).

A ***single*** PC comparison register section 20 and a ***single*** PC latch section 22 being accessible more than once does not amount to plural coincidence detecting circuits.

In ***reversing*** the Board of Patent Appeals and Interferences, the U.S. Court of Appeals for the Federal Circuit explained this axiom within *In re Suitco Surface Inc.*, 94 USPQ2d 1640, 1644 (Fed. Cir. 2010):

> *The broadest-construction rubric coupled with the term "comprising" does not give the PTO an unfettered license to interpret claims to embrace anything remotely related to the claimed invention. Rather, claims should always be **read in light of the specification and teachings in the underlying patent**. See Schriber-Schroth Co. v. Cleveland Trust Co., 311 U.S. 211, 217 [47 USPQ 345] (1940) ("The claims of a patent are always to be read or interpreted in light of its specifications.").*

Page 12 of the Examiner's Answer asserts the following:

> *As pointed out above, the claims are to be given the broadest reasonable interpretation consistent with the specification. See MPEP § 2111. The language of the claims does not limit them to the embodiment shown in Figure 7 of Appellant's specification. Thus, the examiner submits that Suzuki anticipates "a first coincidence detecting circuit" and "a second coincidence detecting circuit" such as recited in claims 65 and 66.*

In response, when the claims are read in the light of the specification the ***meaning of the claims is entirely clear***. *Ex parte Laughlin*, 72 USPQ 391, 393 (Bd. Pat. App. & Int. 1946).

The specification for the claims on appeal at page 24, lines 14-16, provide that as shown in Figure 7, the debugging circuit 100a is constituted by bug address setting registers 110-1 and 110-2 and coincidence detecting circuits 120-1 and 120-2.

However, the Examiner's Answer ***fails*** to highlight any other embodiment within the specification for the claims on appeal having first and second coincidence detecting circuits as claimed being within a single coincidence detecting circuit.

Here, the interpretation of ***first and second*** coincidence detecting circuits being allegedly within Suzuki as contended in the Examiner's Answer ***finds no support*** within Suzuki, and is not a reasonable interpretation under the rules of claim construction. See *In re Vaidyanathan*, 96 USPQ2d 1507, 1516 (Fed. Cir. 2010)(*judgment of the Board is vacated and remanded*).

Thus, Suzuki ***fails to anticipate*** the claims on appeal.

4. For this rejection only, claims 67-68 stand or fall together.

Claim 67 has claim 68 dependent thereon. The Examiner's Answer maintains this rejection of claims 67-68.

Claim 67 is drawn to a data processing apparatus as set forth in claim 66, wherein a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times.	Paragraph beginning at page 25, line 24.

a) Incorporation by reference.

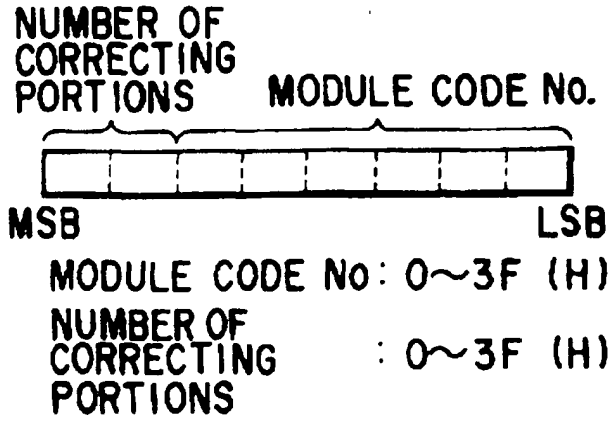
For the purposes of brevity, the arguments presented hereinabove with respect to claim 66 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

b) Page 12 of the Examiner's Answer asserts the following:

In Suzuki, Figure 2B illustrates two bits that are set to a value representing the number of correcting portions in a program module (see, e.g., column 4, lines 41-49).

In response, Figure 2B of Suzuki is provided hereinbelow.



As shown in FIG. 2B, if the lower 6 bits (bit 5 to LSB) are set to a module code No. per one byte and the *residual 2 bits (MSB and bit 6) are set to express the* ***number of correcting portions in the module***, the maximum number of modules to be dealt with becomes 64 (3F (H) to 0 (H)), and the maximum number of correcting portions is four (3 (H) to 0 (H)) (Suzuki at column 4, lines 41-47).

Here, the number of correcting portions in the module depicted within Figure 2B of Suzuki appears to be a ***pre-set*** number.

In this regard, the value of the two most-significant bits shown in Figure 2B of Suzuki is set ***prior to*** performing the process depicted within Figures 4A and 4B,

As a consequence, the value of the number of correcting portions within the two most-significant bits shown in Figure 2B of Suzuki ***appears to be a pre-set value that is not*** based upon any count of the number of times the first or second bug address ***has coincided*** (*not "might coincide"*) with the program address, especially in the absence of any prior comparison between the bug addresses and a program address.

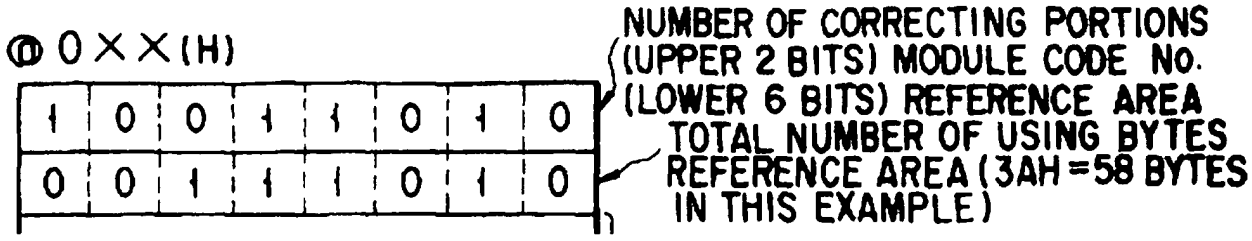
Thus, Suzuki ***fails to anticipate*** the claims on appeal.

c) Page 12 of the Examiner's Answer asserts the following:

> ***Suzuki illustrates that the number of correcting portions, S, is stored in step S5 (see, e.g., FIG. 4A).***

In response, Figure 3 shows an example of a data format reserved in the EEPROM 28 (hereinafter called ROM correction data area) at the time of the interruption processing (Suzuki at column 4, lines 59-61).

A portion of Figure 3 from Suzuki is provided hereinbelow.



Column 6, lines 3-5 of Suzuki provides that the above-obtained number of correction S of code No. m and the head address ("0 xx (H)") of the ROM correction data area are stored (step S5).

Apparently, the values stored within the head address of EEPROM 28 are ***pre-set values*** that are ***not the result*** of the number of times the first and second bug addresses coinciding with the program address.

Here, Suzuki ***fails*** to teach the "*number of use bytes*" and the "*number of times that the first and second bug addresses coincide with the program address*" as being one in the same.

Instead, the "*number of use bytes*" in Suzuki appears to be the "*number of bytes of each correction program*" (Suzuki at column 5, lines 14-18).

Thus, Suzuki ***fails to anticipate*** the claims on appeal.

d) Page 12 of the Examiner's Answer asserts the following:

The ROM correction interruption processing (routine) is executed every time the program counter address coincides with the correction execution interruption address (i.e., the "bug address") of a correcting portion (see, e.g., column 4, lines 12-26 and column 6, lines 27-36).

In response, column 4, lines 12-26 of Suzuki is provided hereinbelow.

> At this time, received/transmitted data is stored in the RAM 16 and the PC value latch section 22 of the ROM correction processing circuit 24 through the internal bus 32 of the microcomputer 12 as required. The PC comparison register section 20 of the ROM correction processing circuit 24 compares a value stored in the PC latch section 22 with an address value (program counter value) of the internal bus 32. Then, if these values are consistent with each other, the PC comparison register section 20 outputs an interruption request signal 34 to the CPU 14. Therefore, if an arbitrary address value for interruption processing is set in the PC value latch section 22 of the ROM correction in advance, interruption processing can be automatically executed to the CPU 14 when the value of the program counter is equal to the value of the PC value latch section 22. In other words, if one ROM correction processing circuit 24 is provided, it is possible to execute the program other than the ROM 18 while the program of the ROM 18 is executing.

However, this passage identified within the Examiner's Answer ***fails*** to disclose, teach, or suggest a number of times first and second bug addresses coincide with the program address is counted, a value representing said number of times. See *Ex parte Darolia*, Appeal No. 2009-005819, pgs. 7-8, (BPAI, June, 2010)(*Examiner's rejection **reversed**: Examiner has not directed Board to any disclosure within the reference*).

Column 6, lines 27-36 of Suzuki is provided hereinbelow.

> In step S11, the main program of the subroutine module of the code No. m is executed at the first time. If the correction execution interruption address set in step S6 is accessed by PC (not shown) during the execution of the main program, the PC comparison register section 20 generates a ROM correction interruption request to the CPU 14. The CPU 14 moves the processing to step 21 to execute the ROM correction interruption processing on the receipt of the request.

However, this passage identified within the Examiner's Answer ***fails*** to disclose, teach, or suggest a number of times first and second bug addresses coincide with the program address is counted, a value representing said number of times. See *Ex parte Darolia*, Appeal No. 2009-005819, pgs. 7-8, (BPAI, June, 2010)(*Examiner's rejection **reversed**: Examiner has not directed Board to any disclosure within the reference*).

Thus, Suzuki ***fails to anticipate*** the claims on appeal.

e) Page 12 of the Examiner's Answer asserts the following:

> ***Then, the stored number of correcting portions S is decremented (see, e.g., step S28 in FIG. 4B and column 6, lines 61-62). In other words, Suzuki teaches "counting down" the stored number of correcting portions S every time the addresses coincide. Thus, Suzuki anticipates the limitation that "a number of times said first and second bug addresses coincide with said program address is counted" such as recited in claim 67.***

Regarding the flowchart in Figure 4B, Suzuki arguably discloses that then, the stored *number of correcting portions S is decremented* (step S28) (Suzuki at column 6, lines 61-62).

*If the number of correcting portions S **is 0***, the processing goes to step S33 since *there is no residual correcting portion* in the subroutine module of code No. m (Suzuki at column 6, lines 65-67).

Furthermore, in step S29, *if the number of correcting portions S is **not 0***, the processing goes to step S30 since there is still residual correcting portions (Suzuki at column 6, line 67 to column 7, line 2).

Here, however, Suzuki ***fails*** to disclose, teach, or suggest the number of correcting portions S representing the number of times that first and second bug addresses coincide with a program address.

Specifically, an Figure 3 with annotations added is provided hereinbelow.

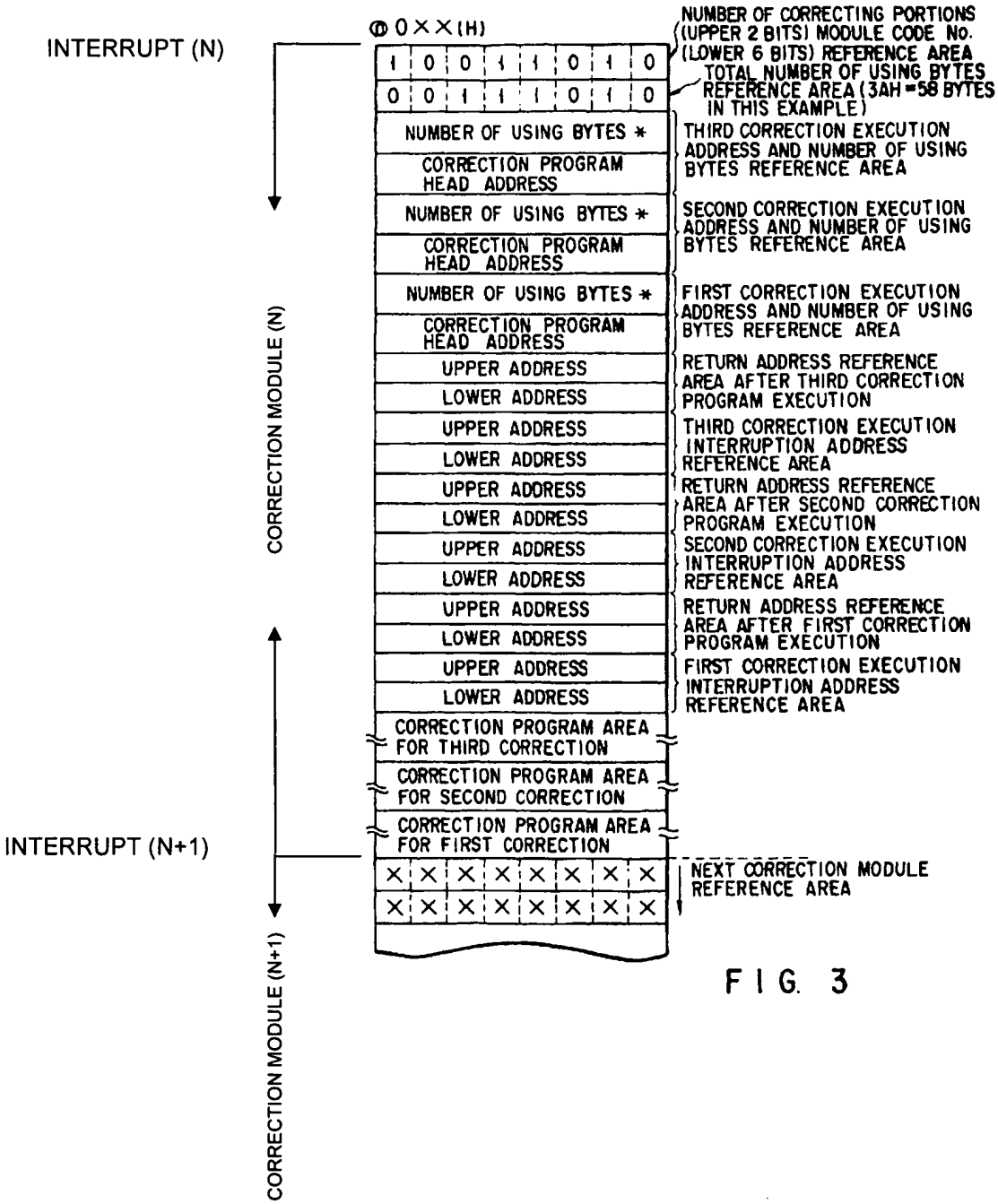


FIG. 3

The PC comparison register section 20 ***generates a ROM correction interruption request*** to the CPU 14 ***in step S11*** of Suzuki, and the CPU 14 moves the processing to step 21 to execute the ROM correction interruption processing on the receipt of the request (Suzuki at Figure 4B, column 6, lines 27-36).

But as shown in Figure 4B, there is ***no count*** within Figure 4A or 4B of Suzuki regarding the number of times that a ROM correction interruption request has been generated.

Instead, the "*number of correcting portions S*" of Suzuki represents the number of correcting portions in a ***single*** module to be corrected (Suzuki at Figure 3).

As a consequence, there is ***no correlation*** within Suzuki between the number of times that a ROM correction interruption request has been generated and the number of correcting portions in a ***single*** module to be corrected.

Thus, Suzuki ***fails to anticipate*** the claims on appeal.

f) Pages 12-13 of the Examiner's Answer assert the following:

The claim further recites "a value representing said number of times." Contrary to Appellant's implication, the examiner does not suggest that the "number of use bytes" described in Suzuki represents the number of times the addresses coincided (brief, page 16). Likewise, the examiner does not suggest that the number of correcting portions S represents the number of times the addresses coincided (brief, page 17). Instead, as set forth in the Office action, the stored number of correcting portions S subtracted from the initial number of correcting portions S represents the number of times the addresses coincided. Thus, Suzuki anticipates "a value representing said number of times" such as recited in the claim.

In response, column 5, lines 14-18, of Suzuki arguably discloses that, however, the number of use bytes marked by "*" in the figure may not be set since the number of bytes of each correction program can be obtained by ***subtracting*** the respective correction program head address values from each other.

Here, Suzuki ***fails*** to disclose, teach, or suggest *the stored number of correcting portions S subtracted from the initial number of correcting portions S representing the number of times the addresses coincided.*

As shown previously within the Appeal Brief and within this Reply Brief, the number of correcting portions S in Suzuki refers to the number of portions to be corrected in a single module.

As shown previously within the Appeal Brief and within this Reply Brief, only one interrupt request is generated in Suzuki for each module that is to be corrected.

As shown in Figure 4B, no additional interrupt request is generated within Suzuki for each of the portion of the module that is corrected.

As a consequence, there is ***no correlation*** within Suzuki between "*the number of times that a ROM correction interruption request has been generated*" and "*the number of correcting portions in a **single** module to be corrected*".

5. For this rejection only, claim 69 stands or falls alone.

The Examiner's Answer maintains this rejection of claim 69.

Claim 69 is drawn to a data processing apparatus as set forth in claim 68, wherein said first buggy part or said second buggy part is selected for correction, said central processing unit (10) using said value to select said first buggy part or said second buggy part.	Paragraph beginning at page 25, line 24.

a) Incorporation by reference.

For the purposes of brevity, the arguments presented hereinabove with respect to claim 67 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

b) Pages 13-14 of the Examiner's Answer assert the following:

However, the examiner does not agree with Appellant's conclusion. In Suzuki, the correcting portions of a program module represent the "buggy parts" of the program module. Suzuki describes that the CPU 14 executes a correction program to correct a selected one of the correcting portions (see, e.g., step S26 in FIG. 4B and column 6, lines 44-57). The correcting portion is selected based on the correction execution interruption address stored in the PC value latch section 22 of the ROM correction processing circuit 24 (see, e.g., column 6, lines 6-11 and 27-36). The correction execution interruption address is stored in the PC value latch section 22 based on the "value" noted above (i.e., the value representing the number of times the addresses coincided).

Suzuki arguably discloses the following in the paragraph beginning at column 6, line 58:

> In the "ROM correction data setting processing for next correcting portion", data of the register such as the accumulator and data of the partial area of the RAM are saved (step S27) similar to step S1. Then, the stored ***number of correcting portions S*** is decremented (step S28). As a result of the decrement, it is checked whether or not the number of correcting portions is 0.

Suzuki arguably discloses the following in the paragraph beginning at column 7, line 7:

> Moreover, the return address to the main program after executing the nth correction program is stored from the EEPROM 28, and stored in the temporarily storing area 42 (step S31). Then, the nth correction program head address and the number of use bytes are read from the EEPROM 28, and the nth correction program is read from the EEPROM based on the ***head address*** and the ***number of use byte*** to be set in the correction execution area of RAM 3 (step S32).

Here, Suzuki ***fails*** to disclose, teach, or suggest the CPU 14 using ***number of correcting portions S*** to select nth correction program head address.

Thus, Suzuki ***fails to anticipate*** the claims on appeal.

C. Rejection of claims 53-57 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,875,342 (Temple).

1. For this rejection only, claims 53-57 stand or fall together.

The Amendment After Final Office Action Under 37 C.F.R. 1.116 includes the cancellation of claims 53-57.

As a consequence, prior claims 53-57 are *no longer the subject of this appeal*.

D. Rejection of claim 54 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,875,342 (Temple).

1. For this rejection only, claim 54 stands or falls alone.

The Amendment After Final Office Action Under 37 C.F.R. 1.116 includes the cancellation of claim 54.

As a consequence, prior claim 54 is *no longer the subject of this appeal*.

E. Rejection of claims 54 and 60-63 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,357,627 (Miyazawa).

1. For this rejection only, claims 54 and 60-62 stand or fall together.

The Amendment After Final Office Action Under 37 C.F.R. 1.116 includes the cancellation of claims 54 and 60-62.

As a consequence, prior claims 54 and 60-62 are *no longer the subject of this appeal*.

2. For this rejection only, claim 63 stands or falls alone.

The Examiner's Answer maintains this rejection of claim 63.

Claim 63 is drawn to a data processing apparatus comprising:	
a central processing unit (10) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (S_A), a first signal (S_{A1}) and a second signal (S_{A2}) being input to said central	Paragraph beginning at page 24, line 25.

processing unit (10) as said interrupt request signal (S_A),	
wherein said central processing unit (10) executes a program code, said program code being stored in memory (50) at a program address,	Paragraph beginning at page 15, line 18.
wherein said memory (50) is random access memory (50),	Paragraph beginning at page 25, line 24.
wherein a counter register is located within said random access memory (50), said counter register being incremented when said program address coincides with a first bug address or a second bug address.	

a) Pages 14-15 of the Examiner's Answer assert the following:

Appellant acknowledges that Suzuki describes that the stored number of correcting portions S is decremented in step S28 (brief, page 25). In other words, Suzuki describes decrementing or counting down a counter or counter register. The stored number of correcting portions S (i.e., the counter register) is decremented in step S28 as part of the "ROM correction data setting processing for [the] next correcting portion" (see, e.g., column 6, lines 58-62), as a result of executing the ROM correction interruption processing (see, e.g., FIG. 4B). As noted above, the ROM correction interruption processing is executed every time the program counter address coincides with the "bug address" of a correcting portion (see, e.g., column 4, lines 12-26 and column 6, lines 27-36). Thus, Suzuki teaches or suggests decrementing a counter register when the program counter address coincides with a bug address.

In response, it is well settled that obviousness requires a suggestion of all limitations in a claim. *Ex parte Bedoukian*, Appeal No. 2010-007177, pg. 3, (BPAI, March, 2011).

Here, there is a ***cooperative relationship between the various elements*** in the claims. *Illinois Tool Works, Inc. v. Continental Can Company, Inc.*, 154 USPQ 401, 420-21 (N.D. Ill. 1967).

Specifically, claim 63 provides for *said counter register being **incremented** when said program address coincides with a first bug address or a second bug address.*

However, either individually or as a whole, Suzuki and Miyazawa are ***silent*** as to a counter register being ***incremented*** when a program address coincides with a first bug address or a second bug address.

Here, not readily apparent is a ***nexus*** between (1) a counter register being ***incremented*** and (2) a program address coinciding with a first bug address or a second bug address. See *In re Jansson*, 203 USPQ 976, 978 (C.C.P.A. 1979)(*rejection **reversed**: attempted nexus is not readily apparent*).

b) Page 15 of the Examiner's Answer asserts the following:

> ***The examiner appreciates that claim 63 recites "said counter register being incremented" rather than decremented. Nonetheless, as reasoned in the Office action, a person of ordinary skill in the art could, with predictable results, implement the data processing apparatus of Suzuki such that the counter register is incremented (i.e., counted up) rather than decremented (i.e., counted down).***

In response, Suzuki is ***silent*** as to *a counter being **incremented** when the program address coincides with a first bug address or a second bug address.*

Likewise, Miyazawa is ***silent*** as to *a counter being **incremented** when the program address coincides with a first bug address or a second bug address.*

In this regard, the Examiner's Answer ***fails*** to identify an instance in Suzuki or Miyazawa of "*a counter being **incremented** when the program address coincides with a first bug address or a second bug address*". *Ex parte Darolia*, Appeal No. 2009-005819, pgs. 7-8, (BPAI, June, 2010)(*rejections **reversed**: Board not directed to any disclosure*).

Nevertheless, in the absence of any disclosure within Suzuki or Miyazawa or any other objective evidence, page 15 of the Examiner's Answer asserts that, *with reference to Figures 4A and 4B of Suzuki, given the number of correcting portions S, a person of ordinary skill in the art could set the initial value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether the stored value is equal to S (rather than 0) in step S29.*

In response, it is respectfully submitted that the Examiner's Answer relies exclusively and extensively upon ***personal conclusions*** in its reasoning.

Rejections on obviousness grounds ***cannot be sustained by mere conclusory statements***; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (U.S. 2007).

Broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

Here, this absence in Suzuki and Miyazawa of "*a counter being **incremented** when the program address coincides with a first bug address or a second bug address*" would have been apparent to the skilled artisan especially when the combination of references would have required a ***substantial reconstruction*** and redesign of the elements shown in Suzuki and Miyazawa, as well as a ***change in the basic principles*** under which the Suzuki and Miyazawa were designed to operate. *In re Ratti*, 123 USPQ 349, 352 (CCPA 1959).

But even if there exists the mere possibility that the features of Suzuki could be so modified or replaced with the features from Miyazawa, as contended within the Office Action, it has been a long standing rule that such modification or replacement ***would not*** make the claimed invention obvious *unless the prior art suggested the desirability of such a modification or replacement*. *In re Brouwer*, 37 USPQ2d 1663, 1666 (Fed. Cir. 1995).

Here, the Examiner's Answer ***fails*** to highlight any *desirability* for connecting for "*a counter being* ***incremented*** *when the program address coincides with a first bug address or a second bug address*". See *Ex parte Rosenfeld*, 130 USPQ 113, 115 (Bd. Pat. App. & Int. 1961)(*decision of the examiner is* ***reversed***).

Determining obviousness requires considering whether two or more pieces of prior art could be combined, or a single piece of prior art could be modified, to produce the claimed invention. *Comaper Corp. v. Antec Inc.*, 93 USPQ2d 1873, 1879 (Fed. Cir. 2010).

Here, the Examiner's Answer ***fails*** to show that "*general conditions*" would have been ***known*** to the skilled artisan. See *In re Yates*, 211 USPQ 1149 (C.C.P.A. 1981). See also *In re Orfeo and Murphy*, 169 USPQ 487 (C.C.P.A. 1971).

Obviousness cannot be predicated on what is unknown. *In re Spormann*, 150 USPQ 449, 452 (CCPA 1966).

One cannot choose from the unknown. *In re Ochiai*, 37 USPQ2d 1127, 1131 (Fed. Cir. 1995).

There must be a reason apparent at the time the invention was made to the person of ordinary skill in the art for applying the teaching at hand, or the use of the teaching as evidence of obviousness will entail prohibited hindsight. *In re Nomiya, Kohisa, and Matsumura*, 184 USPQ 607, 613 (C.C.P.A. 1975).

Prima facie obviousness of a claimed invention is established "only by showing some ***objective teaching in the prior art*** or that ***knowledge*** generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

There must be a reason or suggestion in the art for selecting the procedure used, other than the knowledge learned from the applicant's disclosure. *Interconnect Planning Corporation v. Feil*, 227 USPQ 543,551 (Fed. Cir. 1985).

A ***piecemeal reconstruction*** of prior art elements ***absent some suggestion*** of the combination ***does not show obviousness***. *Independent Products Co. v. Tamor Plastics Corp.*, 19 USPQ2d 1314, 1315-16 (Fed. Cir. 1991).

Such a ***hindsight analysis is not allowed*** by 35 U.S.C. 103 which requires a comparison of the prior art and the invention as a whole at the time the invention was made. *In re Linnert and Espy*, 135 USPQ 307, 311 (C.C.P.A. 1962).

To imbue one of ordinary skill in the art with knowledge of the invention, when ***no prior art reference or references of record convey or suggest that knowledge***, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 USPQ 303, 312-313 (Fed. Cir. 1983).

The specification for the claims on appeal provides the following in the paragraph beginning at page 25, line 24:

> Here, in order to execute a plurality of debugged programs in an appropriate order, a branch processing program is provided at the start of the interrupt processing routine for branching to each debugged program. For example, a predetermined memory address is assigned as a counter register in the RAM 50. At the initialization, the counter register is cleared (is set to 0). Each time an interrupt routine is executed, ***the counter register is increased by 1***. The CPU 10 is able to judge the number of times of interrupt, that is, which number bug is being corrected, by the value of the counter register. Therefore, the CPU 10 is able to branch to the correct debugged program accordingly, read the program code, and perform the predetermined processing.

In the absence of any disclosure within Suzuki or Mabuchi, or any other objective supporting evidence, the line of reasoning within the Examiner's Answer appears to have been merely ***an extraction from the Appellant's own specification***.

Under similar circumstances, Judge Frankfort of the Board of Patent Appeals and Interferences provides guidance in *Ex parte Haymond*, 41 USPQ2d 1217, 1220 (Bd. Pat. App. & Int. 1996), as follows:

> [3] In this regard, we note that it is ***impermissible*** to use the claimed invention as an instruction manual or "template" to piece together isolated disclosures and teachings of the prior art so that the claimed invention may be rendered obvious. We additionally note that a rejection based on Section 103 must rest on a factual basis, with the facts being interpreted without hindsight reconstruction of the invention from the prior art. In making this evaluation, the examiner has the initial duty of supplying the factual basis for the rejection he advances. He *may not*, because he doubts that the invention is patentable, resort to ***speculation***, ***unfounded assumptions*** or ***hindsight reconstruction*** to supply deficiencies in the factual basis. See *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968). Since we perceive ***no factual basis*** *in the prior art relied upon which supports the proposed combination* thereof, and have thus determined that the examiner's conclusion of obviousness is based on *hindsight reconstruction* of the claimed invention from isolated disparate teachings in the prior art, ***we will not sustain*** the examiner's rejection of appealed claims 1, 3 and 4 under 35 U.S.C. Section 103.

But instead of providing any objective evidence for showing motivation or desirability, the Office Action relies upon impermissible ***hindsight reconstruction*** to arrive at the determination of obviousness.

It is ***impermissible*** simply to engage in a ***hindsight reconstruction*** of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. *In re Gorman*, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991).

Thus, the Examiner's Answer ***fails*** provide any objective evidence sufficient for showing the desirability of the modifying or replacing the features of Suzuki or Miyazawa.

Instead, page 15 of the Examiner's Answer asserts that ***such an implementation is analogous to the one described in Suzuki and provides the intended results***.

However, the Examiner's Answer ***fails*** to particularly identify any *result that is intended.*

Likewise, the Examiner's Answer ***fails*** to particularly identify any *feature or step within Suzuki or Miyazawa that would affect that unspecified result.*

The ***rejection here runs afoul*** of a basis mandate inherent in §103- that a ***piecemeal reconstruction*** of the prior art patents in the light of appellants' disclosure ***shall not*** be the basis for a holding of obviousness. *In re Kamm and Young*, 172 USPQ 298, 301 (C.C.P.A. 1972).

c) Page 16 of the Examiner's Answer asserts the following:

> ***The examiner respectfully submits that Appellant's citation to Ex parte Givens is misplaced (brief, page 26). The decision in Ex parte Givens and the explanation that "a summer is an additive circuit and not a subtractive circuit" relate to adaptive filtering algorithms, not to incrementing and decrementing operations. Moreover, the decision in Ex parte Givens relates to anticipation and not to obviousness.***

In response, *Ex parte Givens*, Appeal No. 2009-003414, pg. 3 (BPAI, August 6, 2009) addresses the issue of an unreasonably broad claim construction relied upon in the rejection of the claims in that appeal.

As explained by Judge Krivak of the Board of Patent Appeals and Interferences in *Ex parte Givens*, "*a summer is an additive circuit and **not** a subtractive circuit*.

Claim 63 on appeal in the instant application provides for *said counter register **being incremented** when said program address coincides with a first bug address or a second bug address.*

Each time an interrupt routine is executed, ***the counter register is increased by 1*** (Specification at page 26, lines 6-7).

Regarding the flowchart in Figure 4B, Suzuki arguably discloses that then, the stored *number of correcting portions S is **decremented*** (step S28) (Suzuki at column 6, lines 61-62).

Whereas "*a summer is an additive circuit and **not** a subtractive circuit*" as explained by Judge Krivak in *Ex parte Givens*, reliance upon the ***decrementing*** in step 28 of Suzuki for the ***incrementing*** in claim 63 is in the same way ***unreasonable***. *In re Suitco Surface Inc.*, 94 USPQ2d 1640, 1644 (Fed. Cir. 2010)(*PTO's construction is **unreasonably broad***).

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

The prior art of record fails to disclose, teach or suggest all the features of the claimed invention.

For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection of the claims on appeal is respectfully requested.

Dated: July 12, 2011

Respectfully submitted,

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CLAIMS APPENDIX

1-62. (Canceled)

63. A data processing apparatus comprising:

a central processing unit configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal, a first signal and a second signal being input to said central processing unit as said interrupt request signal,

wherein said central processing unit executes a program code, said program code being stored in memory at a program address,

wherein said memory is random access memory,

wherein a counter register is located within said random access memory, said counter register being incremented when said program address coincides with a first bug address or a second bug address.

64. A data processing apparatus comprising:

a central processing unit configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal, a first signal and a second signal being input to said central processing unit as said interrupt request signal,

wherein said central processing unit executes a program code, said program code being stored in memory at a program address,

wherein said first signal indicates when said program address and a first bug address coincide, said second signal indicating when said program address and a second bug address coincide.

65. A data processing apparatus as set forth in claim 64, wherein a first coincidence detecting circuit compares said program address with said first bug address, said first coincidence detecting circuit outputting said first signal when said program address and said first bug address coincide.

66. A data processing apparatus as set forth in claim 65, wherein a second coincidence detecting circuit compares said program address with said second bug address, said second coincidence detecting circuit outputting said second signal when said program address and said second bug address coincide.

67. A data processing apparatus as set forth in claim 66, wherein a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times.

68. A data processing apparatus as set forth in claim 67, wherein said first bug address indicates a starting address for a first buggy part of a program or data, said second bug address indicating a starting address for a second buggy part of said program or data.

69. A data processing apparatus as set forth in claim 68, wherein said first buggy part or said second buggy part is selected for correction, said central processing unit using said value to select said first buggy part or said second buggy part.